PicoCode Map

Low Order Byte of Address

High Order Byte of Address	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	00 0A 00 07	00 10 00 08	00 00 04 3F													00 00 00 00
1	04 05 D0 00	01 0C D0 40														00 0A 00 46
2	00 02 D0 00															00 0A 00 C6
3	06 85 48 00	01 08 D0 C0														00 0A 00 C6
4	01 08 D1 07	0D 24 F8 00														00 0A 01 00
5	06 C5 48 00	01 0C F9 40														00 0A 01 46
6	00 00 00 00	00 02 D0 00														00 0A 01 82
7	06 05 30 00	01 08 D1 C0														00 0A 01 C6
8	00 00 00 00	00 02 D0 00														00 0A 02 01
9	06 C5 30 00	01 08 D2 40														00 0A 02 46
A																04 05 00 00
B																04 85 78 00
C	04 05 D8 00	01 08 D3 00														00 0A 03 06
D	04 05 F0 00	01 08 D3 40														00 0A 03 46
E	04 05 B0 00	01 08 D3 80														00 0A 03 86
F	02 80 98 00	02 00 98 00														00 00 03 C6

Mnemonic	Op Code	Operand	Addressing Mode	Mnemonic	Op Code	Operand	Addressing Mode		Affected ZL	Affected CL	Instruction
NOP	00	—	Inherent	—	—	———	———		—	—	No Operation
LDA	10	Data	Immediate	LDA	11	Data Addr	Direct		↕	—	Load Accumulator
—	—	—	———	BRA	20	Branch Addr	Direct		—	—	Branch Always
ADD	30	Data	Immediate	ADD	31	Data Addr	Direct	No Carry	↕	↕	Add to Accumulator without Carry Latch
—	—	—	———	STA	40	Data Addr	Direct		↕	—	Store Accumulator to RAM
ADC	50	Data	Immediate	ADC	51	Data Addr	Direct	With Carry	↕	↕	Add to Accumulator with Carry Latch
—	—	—	———	BRZ	60	Branch Addr	Direct		—	—	Branch if Zero Latch Set
SUB	70	Data	Immediate	SUB	71	Data Addr	Direct	No Carry	↕	↕	Subtract from Accumulator without Carry Latch
—	—	—	———	BCS	80	Branch Addr	Direct		—	—	Branch if Carry Latch Set
SBC	90	Data	Immediate	SBC	91	Data Addr	Direct	With Carry	↕	↕	Subtract from Accumulator with Carry Latch
INC	A0	—	Inherent						↕	—	Increment Accumulator
DEC	B0	—	Inherent						↕	—	Decrement Accumulator
AND	C0	Data	Immediate	AND	C1	Data Addr	Direct	Logic	↕	—	And Data with Accumulator
ORA	D0	Data	Immediate	ORA	D1	Data Addr	Direct	Logic	↕	—	Or Data with Accumulator
EOR	E0	Data	Immediate	EOR	E1	Data Addr	Direct	Logic	↕	—	Exclusive Or Data with Accumulator
CLC	F0	—	Inherent	SEC	F1	———	Inherent		—	↕	Clear Carry Latch, Set Carry Latch

Not Implemented

INC	A1	Data Addr	Direct	No Carry
DEC	B1	Data Addr	Direct	No Carry

Approvals	Date	Title:	
Drawn:		Size:	Part Number: Rev.
Checked:		Scale:	Sheet: 1 of 10
Approved:			

ROM Contents

Module3

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	00	00	00													00
1	04	01														00
2	00															00
3	06	01														00
4	01	0D														00
5	06	01														00
6	00	00														00
7	06	01														00
8	00	00														00
9	06	01														00
A																04
B																04
C	04	01														00
D	04	01														00
E	04	01														00
F	02	02														00

Module2

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	0A	10	00													00
1	05	08														0A
2	02															0A
3	85	08														0A
4	08	24														0A
5	C5	08														0A
6	00	02														0A
7	05	08														0A
8	00	02														0A
9	C5	08														0A
A																05
B																85
C	05	08														0A
D	05	08														0A
E	05	08														0A
F	80	00														00

Module1

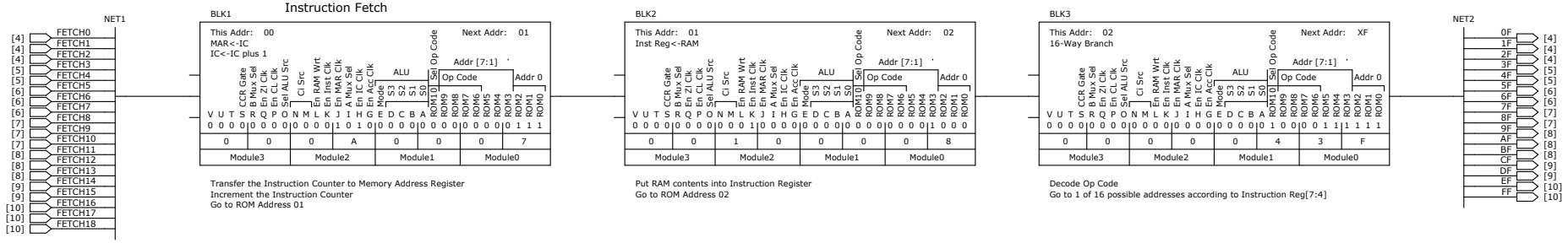
	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	00	00	04													00
1	D0	D0														00
2	D0															00
3	48	D0														00
4	D1	F8														01
5	48	D1														01
6	00	D0														01
7	30	D1														01
8	00	D0														02
9	30	D2														02
A																00
B																78
C	D8	D3														03
D	F0	D3														03
E	B0	D3														03
F	98	98														03

Module0

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	07	08	3F													00
1	00	40														46
2	00															80
3	00	C0														C6
4	07	00														00
5	00	40														46
6	00	00														82
7	00	C0														C6
8	00	00														01
9	00	40														46
A																00
B																00
C	00	00														06
D	00	40														46
E	00	80														86
F	00	00														C6

Part Number:

Instruction Fetch

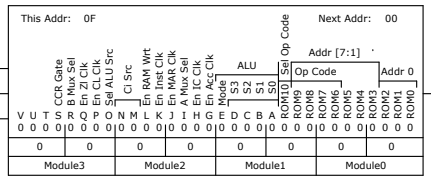


Part Number:

Sheet: 3 of 10

No Operation

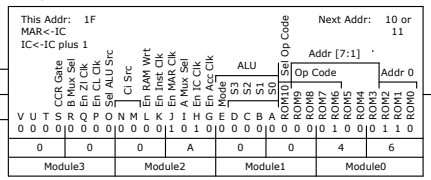
BLK4



Go to ROM Address 00

Load Accumulator

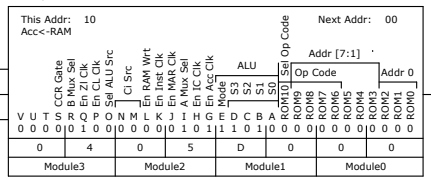
BLK5



Transfer the Instruction Counter to Memory Address Register
Increment the Instruction Counter
Test OP0 and go to ROM Address 10 or 11

Immediate

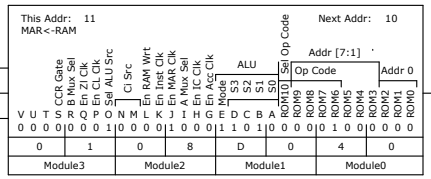
BLK6



Transfer RAM data to Accumulator
Go to ROM Address 00

Direct

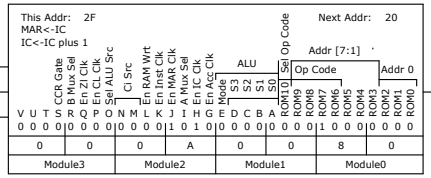
BLK7



Transfer RAM data to Memory Address Register
Go to ROM Address 10

Branch Always

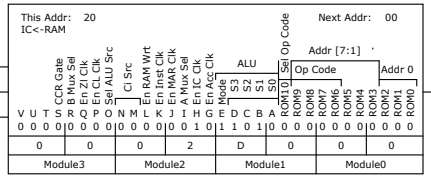
BLK8



Transfer the Instruction Counter to Memory Address Register
Increment the Instruction Counter
Go to ROM Address 20

Direct

BLK9



Transfer RAM data to nstruction Counter
Go to ROM Address 00

Part Number:	
Sheet:	4 of 10

Part Number:	
Sheet:	5 of 10

Add With Carry

BLK16

This Addr: 5F
MAR<-IC
IC<-IC plus 1

Next Addr: 50 or 51

[3] 5F

V	U	T	S	R	Q	P	O	N	M	L	K	J	I	H	G	E	D	C	B	A	ROM10	ROM9	ROM8	ROM7	ROM6	ROM5	ROM4	ROM3	ROM2	ROM1	ROM0
0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	1	1	0

Op Code: Sel
ALU: Mode, S3, S2, S1, S0
En Acc Clk, En IC Clk, En A Mux Sel, En MAR Clk, En Inst Clk, En RAM Wrt, CI Src, Sel ALU Src, En CL Clk, En ZI Clk, En B Mux Sel, CCR Gate
Addr [7:1]: Op Code
Addr 0

0	0	0	A	0	1	4	6
Module3		Module2		Module1		Module0	

Transfer the Instruction Counter to Memory Address Register
Increment the Instruction Counter
Go to ROM Address 50 or 51

Immediate

BLK17

This Addr: 50
Acc<-Acc plus RAM plus Carry Latch

Next Addr: 00

V	U	T	S	R	Q	P	O	N	M	L	K	J	I	H	G	E	D	C	B	A	ROM10	ROM9	ROM8	ROM7	ROM6	ROM5	ROM4	ROM3	ROM2	ROM1	ROM0
0	0	0	0	0	1	1	0	0	1	1	0	0	1	0	1	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0

Op Code: Sel
ALU: Mode, S3, S2, S1, S0
En Acc Clk, En IC Clk, En A Mux Sel, En MAR Clk, En Inst Clk, En RAM Wrt, CI Src, Sel ALU Src, En CL Clk, En ZI Clk, En B Mux Sel, CCR Gate
Addr [7:1]: Op Code
Addr 0

0	6	C	5	4	8	0	0
Module3		Module2		Module1		Module0	

FETCH5 [3]

Add Accumulator to RAM data and put in Accumulator
Go to ROM Address 00

Direct

BLK18

This Addr: 51
MAR<-RAM

Next Addr: 50

V	U	T	S	R	Q	P	O	N	M	L	K	J	I	H	G	E	D	C	B	A	ROM10	ROM9	ROM8	ROM7	ROM6	ROM5	ROM4	ROM3	ROM2	ROM1	ROM0
0	0	0	0	0	0	0	0	1	0	0	0	0	1	0	0	1	1	0	1	0	0	0	0	1	0	1	0	0	0	0	0	0

Op Code: Sel
ALU: Mode, S3, S2, S1, S0
En Acc Clk, En IC Clk, En A Mux Sel, En MAR Clk, En Inst Clk, En RAM Wrt, CI Src, Sel ALU Src, En CL Clk, En ZI Clk, En B Mux Sel, CCR Gate
Addr [7:1]: Op Code
Addr 0

0	1	0	8	D	1	4	0
Module3		Module2		Module1		Module0	

Transfer RAM data to Memory Address Register
Go to ROM Address 50

Branch IF Zero Latch Set

BLK19

This Addr: 6F
MAR<-IC
IC<-IC plus 1

Next Addr: 60 or 61

[3] 6F

V	U	T	S	R	Q	P	O	N	M	L	K	J	I	H	G	E	D	C	B	A	ROM10	ROM9	ROM8	ROM7	ROM6	ROM5	ROM4	ROM3	ROM2	ROM1	ROM0
0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0	0

Op Code: Sel
ALU: Mode, S3, S2, S1, S0
En Acc Clk, En IC Clk, En A Mux Sel, En MAR Clk, En Inst Clk, En RAM Wrt, CI Src, Sel ALU Src, En CL Clk, En ZI Clk, En B Mux Sel, CCR Gate
Addr [7:1]: Op Code
Addr 0

0	0	0	A	0	1	8	2
Module3		Module2		Module1		Module0	

Transfer the Instruction Counter to Memory Address Register
Increment the Instruction Counter
Go to ROM Address 60 or 61

No Branch

BLK20

This Addr: 60
NOP

Next Addr: 00

V	U	T	S	R	Q	P	O	N	M	L	K	J	I	H	G	E	D	C	B	A	ROM10	ROM9	ROM8	ROM7	ROM6	ROM5	ROM4	ROM3	ROM2	ROM1	ROM0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Op Code: Sel
ALU: Mode, S3, S2, S1, S0
En Acc Clk, En IC Clk, En A Mux Sel, En MAR Clk, En Inst Clk, En RAM Wrt, CI Src, Sel ALU Src, En CL Clk, En ZI Clk, En B Mux Sel, CCR Gate
Addr [7:1]: Op Code
Addr 0

0	0	0	0	0	0	0	0
Module3		Module2		Module1		Module0	

FETCH6 [3]

Go to ROM Address 00

Direct

BLK21

This Addr: 61
IC<-RAM

Next Addr: 00

V	U	T	S	R	Q	P	O	N	M	L	K	J	I	H	G	E	D	C	B	A	ROM10	ROM9	ROM8	ROM7	ROM6	ROM5	ROM4	ROM3	ROM2	ROM1	ROM0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0

Op Code: Sel
ALU: Mode, S3, S2, S1, S0
En Acc Clk, En IC Clk, En A Mux Sel, En MAR Clk, En Inst Clk, En RAM Wrt, CI Src, Sel ALU Src, En CL Clk, En ZI Clk, En B Mux Sel, CCR Gate
Addr [7:1]: Op Code
Addr 0

0	0	0	2	D	0	0	0
Module3		Module2		Module1		Module0	

FETCH7 [3]

Transfer RAM data to nstruction Counter
Go to ROM Address 00

Part Number:

Sheet: 6 of 10

Sutract Without Carry

BLK22

This Addr: 7F
MAR<-IC
IC<-IC plus 1

Next Addr: 70 or 71

[3] 7F

V	U	T	S	R	Q	P	O	N	M	L	K	J	I	H	G	E	D	C	B	A	ROM10	ROM9	ROM8	ROM7	ROM6	ROM5	ROM4	ROM3	ROM2	ROM1	ROM0
0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	1	1	0

CCR Gate, B Mux Sel, En ZI Clk, En CL Clk, Sel ALU Src, CI Src, En RAM Wrt, En Inst Clk, En MAR Clk, A Mux Sel, En IC Clk, En Acc Clk, ALU Mode, ALU S3, ALU S2, ALU S1, ALU S0, Op Code Sel, Op Code, Addr [7:1], Addr 0

0	0	0	A	0	1	C	6
Module3		Module2		Module1		Module0	

Transfer the Instruction Counter to Memory Address Register
Increment the Instruction Counter
Go to ROM Address 70 or 71

Immediate

BLK23

This Addr: 70
Acc<-Acc minus RAM

Next Addr: 00

FETCH8 [3]

V	U	T	S	R	Q	P	O	N	M	L	K	J	I	H	G	E	D	C	B	A	ROM10	ROM9	ROM8	ROM7	ROM6	ROM5	ROM4	ROM3	ROM2	ROM1	ROM0
0	0	0	0	0	1	1	0	0	0	0	0	0	1	0	1	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0

CCR Gate, B Mux Sel, En ZI Clk, En CL Clk, Sel ALU Src, CI Src, En RAM Wrt, En Inst Clk, En MAR Clk, A Mux Sel, En IC Clk, En Acc Clk, ALU Mode, ALU S3, ALU S2, ALU S1, ALU S0, Op Code Sel, Op Code, Addr [7:1], Addr 0

0	6	0	5	3	0	0	0
Module3		Module2		Module1		Module0	

Subtract RAM from Accumulator and put in Accumulator
Go to ROM Address 00

Direct

BLK24

This Addr: 71
MAR<-RAM

Next Addr: 70

V	U	T	S	R	Q	P	O	N	M	L	K	J	I	H	G	E	D	C	B	A	ROM10	ROM9	ROM8	ROM7	ROM6	ROM5	ROM4	ROM3	ROM2	ROM1	ROM0
0	0	0	0	0	0	0	1	0	0	0	0	1	0	0	0	1	1	0	1	0	0	0	0	1	1	1	0	0	0	0	0	0

CCR Gate, B Mux Sel, En ZI Clk, En CL Clk, Sel ALU Src, CI Src, En RAM Wrt, En Inst Clk, En MAR Clk, A Mux Sel, En IC Clk, En Acc Clk, ALU Mode, ALU S3, ALU S2, ALU S1, ALU S0, Op Code Sel, Op Code, Addr [7:1], Addr 0

0	1	0	8	D	1	C	0
Module3		Module2		Module1		Module0	

Transfer RAM data to Memory Address Register
Go to ROM Address 70

Branch IF Carry Latch Set

BLK25

This Addr: 8F
MAR<-IC
IC<-IC plus 1

Next Addr: 80 or 81

[3] 8F

V	U	T	S	R	Q	P	O	N	M	L	K	J	I	H	G	E	D	C	B	A	ROM10	ROM9	ROM8	ROM7	ROM6	ROM5	ROM4	ROM3	ROM2	ROM1	ROM0
0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1

CCR Gate, B Mux Sel, En ZI Clk, En CL Clk, Sel ALU Src, CI Src, En RAM Wrt, En Inst Clk, En MAR Clk, A Mux Sel, En IC Clk, En Acc Clk, ALU Mode, ALU S3, ALU S2, ALU S1, ALU S0, Op Code Sel, Op Code, Addr [7:1], Addr 0

0	0	0	A	0	2	0	1
Module3		Module2		Module1		Module0	

Transfer the Instruction Counter to Memory Address Register
Increment the Instruction Counter
Go to ROM Address 80 or 81

No Branch

BLK26

This Addr: 80
NOP

Next Addr: 00

FETCH9 [3]

V	U	T	S	R	Q	P	O	N	M	L	K	J	I	H	G	E	D	C	B	A	ROM10	ROM9	ROM8	ROM7	ROM6	ROM5	ROM4	ROM3	ROM2	ROM1	ROM0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

CCR Gate, B Mux Sel, En ZI Clk, En CL Clk, Sel ALU Src, CI Src, En RAM Wrt, En Inst Clk, En MAR Clk, A Mux Sel, En IC Clk, En Acc Clk, ALU Mode, ALU S3, ALU S2, ALU S1, ALU S0, Op Code Sel, Op Code, Addr [7:1], Addr 0

0	0	0	0	0	0	0	0
Module3		Module2		Module1		Module0	

Go to ROM Address 00

Direct

BLK27

This Addr: 81
IC<-RAM

Next Addr: 00

FETCH10 [3]

V	U	T	S	R	Q	P	O	N	M	L	K	J	I	H	G	E	D	C	B	A	ROM10	ROM9	ROM8	ROM7	ROM6	ROM5	ROM4	ROM3	ROM2	ROM1	ROM0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0

CCR Gate, B Mux Sel, En ZI Clk, En CL Clk, Sel ALU Src, CI Src, En RAM Wrt, En Inst Clk, En MAR Clk, A Mux Sel, En IC Clk, En Acc Clk, ALU Mode, ALU S3, ALU S2, ALU S1, ALU S0, Op Code Sel, Op Code, Addr [7:1], Addr 0

0	0	0	2	D	0	0	0
Module3		Module2		Module1		Module0	

Transfer RAM data to nstruction Counter
Go to ROM Address 00

Part Number:	
Sheet:	7 of 10

Sutract With Carry

BLK28

This Addr: 9F
MAR<-IC
IC<-IC plus 1

Next Addr: 90 or 91

[3] 9F

V	U	T	S	R	Q	P	O	N	M	L	K	J	I	H	G	E	D	C	B	A	ROM10	ROM9	ROM8	ROM7	ROM6	ROM5	ROM4	ROM3	ROM2	ROM1	ROM0
0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	1	1	0

Op Code, Addr [7:1], Addr 0; CCR Gate, B Mux Sel, En ZI Clk, En CL Clk, Sel ALU Src, CI Src, En RAM Wrt, En Inst Clk, En MAR Clk, A Mux Sel, En IC Clk, En Acc Clk, ALU (Mode, S3, S2, S1, S0), Sel

0	0	0	A	0	2	4	6
Module3		Module2		Module1		Module0	

Transfer the Instruction Counter to Memory Address Register
Increment the Instruction Counter
Go to ROM Address 90 or 91

Immediate

BLK29

This Addr: 90
Acc<-Acc minus RAM minus Carry

Next Addr: 00

V	U	T	S	R	Q	P	O	N	M	L	K	J	I	H	G	E	D	C	B	A	ROM10	ROM9	ROM8	ROM7	ROM6	ROM5	ROM4	ROM3	ROM2	ROM1	ROM0
0	0	0	0	0	1	1	0	1	1	1	0	0	1	0	1	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0

Op Code, Addr [7:1], Addr 0; CCR Gate, B Mux Sel, En ZI Clk, En CL Clk, Sel ALU Src, CI Src, En RAM Wrt, En Inst Clk, En MAR Clk, A Mux Sel, En IC Clk, En Acc Clk, ALU (Mode, S3, S2, S1, S0), Sel

0	6	C	5	3	0	0	0
Module3		Module2		Module1		Module0	

FETCH11 [3]

Subtract RAM from Accumulator minus Carry and put in Accumulator
Go to ROM Address 00

Direct

BLK30

This Addr: 91
MAR<-RAM

Next Addr: 90

V	U	T	S	R	Q	P	O	N	M	L	K	J	I	H	G	E	D	C	B	A	ROM10	ROM9	ROM8	ROM7	ROM6	ROM5	ROM4	ROM3	ROM2	ROM1	ROM0
0	0	0	0	0	0	0	1	0	0	0	0	1	0	0	0	1	1	0	1	0	0	0	1	0	0	1	0	0	0	0	0

Op Code, Addr [7:1], Addr 0; CCR Gate, B Mux Sel, En ZI Clk, En CL Clk, Sel ALU Src, CI Src, En RAM Wrt, En Inst Clk, En MAR Clk, A Mux Sel, En IC Clk, En Acc Clk, ALU (Mode, S3, S2, S1, S0), Sel

0	1	0	8	D	2	4	0
Module3		Module2		Module1		Module0	

Transfer RAM data to Memory Address Register
Go to ROM Address 90

Increment Accumulator

BLK31

This Addr: AF
Acc<-Acc plus 1

Next Addr: 00

[3] AF

V	U	T	S	R	Q	P	O	N	M	L	K	J	I	H	G	E	D	C	B	A	ROM10	ROM9	ROM8	ROM7	ROM6	ROM5	ROM4	ROM3	ROM2	ROM1	ROM0
0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Op Code, Addr [7:1], Addr 0; CCR Gate, B Mux Sel, En ZI Clk, En CL Clk, Sel ALU Src, CI Src, En RAM Wrt, En Inst Clk, En MAR Clk, A Mux Sel, En IC Clk, En Acc Clk, ALU (Mode, S3, S2, S1, S0), Sel

0	4	0	5	0	0	0	0
Module3		Module2		Module1		Module0	

FETCH12 [3]

Increment Accumulator and put in Accumulator
Go to ROM Address 00

Decrement Accumulator

BLK32

This Addr: BF
Acc<-Acc minus 1

Next Addr: 00

[3] BF

V	U	T	S	R	Q	P	O	N	M	L	K	J	I	H	G	E	D	C	B	A	ROM10	ROM9	ROM8	ROM7	ROM6	ROM5	ROM4	ROM3	ROM2	ROM1	ROM0
0	0	0	0	0	1	0	0	1	0	0	0	0	1	0	1	0	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0

Op Code, Addr [7:1], Addr 0; CCR Gate, B Mux Sel, En ZI Clk, En CL Clk, Sel ALU Src, CI Src, En RAM Wrt, En Inst Clk, En MAR Clk, A Mux Sel, En IC Clk, En Acc Clk, ALU (Mode, S3, S2, S1, S0), Sel

0	4	8	5	7	8	0	0
Module3		Module2		Module1		Module0	

FETCH13 [3]

Decrement Accumulator and put in Accumulator
Go to ROM Address 00

Part Number:	
Sheet:	8 of 10

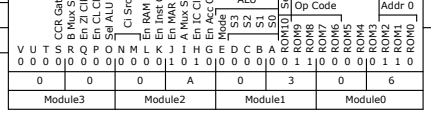
AND Accumulator with Data

BLK33

This Addr: CF
MAR<-IC
IC<-IC plus 1

Next Addr: C0 or C1

[3] CF



0	0	0	A	0	3	0	6
Module3		Module2		Module1		Module0	

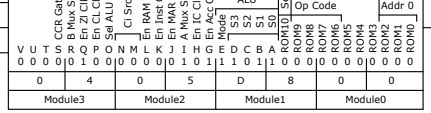
Transfer the Instruction Counter to Memory Address Register
Increment the Instruction Counter
Go to ROM Address C0 or C1

Immediate

BLK34

This Addr: C0
Acc<-Acc AND RAM

Next Addr: 00



0	4	0	5	D	8	0	0
Module3		Module2		Module1		Module0	

Accumulator AND RAM Data put in Accumulator
Go to ROM Address 00

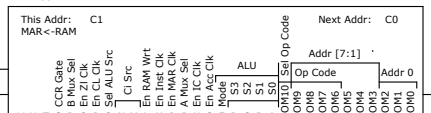
FETCH14 [3]

Direct

BLK35

This Addr: C1
MAR<-RAM

Next Addr: C0



0	1	0	8	D	3	0	0
Module3		Module2		Module1		Module0	

Transfer RAM data to Memory Address Register
Go to ROM Address C0

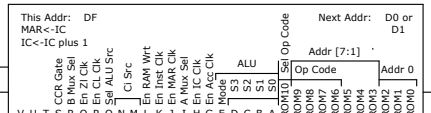
OR Accumulator with Data

BLK36

This Addr: DF
MAR<-IC
IC<-IC plus 1

Next Addr: D0 or D1

[3] DF



0	0	0	A	0	3	4	6
Module3		Module2		Module1		Module0	

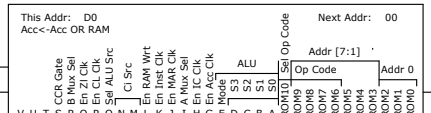
Transfer the Instruction Counter to Memory Address Register
Increment the Instruction Counter
Go to ROM Address D0 or D1

Immediate

BLK37

This Addr: D0
Acc<-Acc OR RAM

Next Addr: 00



0	4	0	5	F	0	0	0
Module3		Module2		Module1		Module0	

Accumulator OR RAM Data put in Accumulator
Go to ROM Address 00

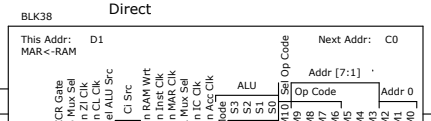
FETCH15 [3]

Direct

BLK38

This Addr: D1
MAR<-RAM

Next Addr: C0



0	1	0	8	D	3	4	0
Module3		Module2		Module1		Module0	

Transfer RAM data to Memory Address Register
Go to ROM Address D0

Part Number:

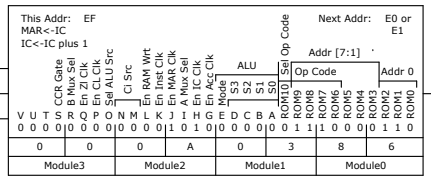
Sheet: 9 of 10

EOR Accumulator with Data

BLK39

This Addr: EF
MAR<-IC
IC<-IC plus 1

Next Addr: E0 or E1



[3] EF

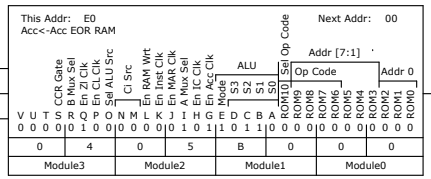
Transfer the Instruction Counter to Memory Address Register
Increment the Instruction Counter
Go to ROM Address E0 or E1

Immediate

BLK40

This Addr: E0
Acc<-Acc EOR RAM

Next Addr: 00



FETCH16 [3]

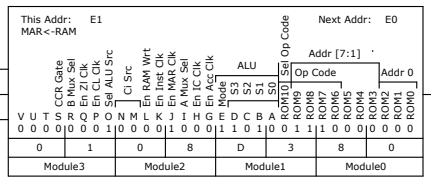
Accumulator EOR RAM Data put in Accumulator
Go to ROM Address 00

Direct

BLK41

This Addr: E1
MAR<-RAM

Next Addr: E0



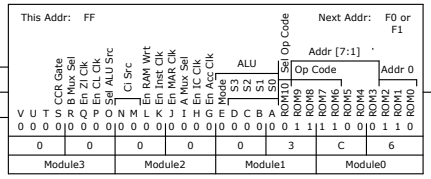
Transfer RAM data to Memory Address Register
Go to ROM Address E0

Clear/Set Carry Latch

BLK42

This Addr: FF

Next Addr: F0 or F1



[3] FF

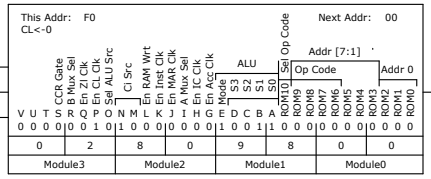
Increment Accumulator and put in Accumulator
Go to ROM Address 00

Clear Carry Latch

BLK43

This Addr: F0
CL<-0

Next Addr: 00



FETCH17 [3]

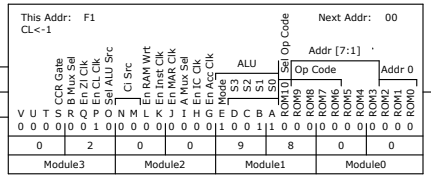
Clear Carry Latch
Go to ROM Address 00

Set Carry Latch

BLK44

This Addr: F1
CL<-1

Next Addr: 00



FETCH18 [3]

Set Carry Latch
Go to ROM Address 00

Part Number:	
Sheet:	10 of 10