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S1V30120
Hardware Specification

SEIKO EPSON CORPORATION

Rev.1.2

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1. Outline

The S1V30120 is a Speech Synthesis IC that provides a cost effective solution for adding Text-To-Speech (TTS) and ADPCM speech processing applications to a range of portable devices. The highly integrated design reduces overall system cost and time-to-market. The S1V30120 contains all the required analogue codecs, memory, and EPSON-supplied embedded algorithms. All applications are controlled over a single serial interface (SPI) allowing control from a wide range of hosts and rapid integration into existing products.

2. Features

- Text To Speech Synthesis (TTS)
  - Fonix DECtalk® v5, fully parametric speech synthesis
  - Languages: US English, Castilian Spanish, Latin American Spanish
  - Nine pre-defined voices
  - Sampling rate: 11.025kHz
- Audio reproduction (ADPCM)
  - ADPCM decoding (in Epson's original format)
  - Bit rate: 80kbps, 64kbps, 48kbps, 40kbps, 32kbps and 24kbps
  - Sampling rate: 16, 8 kHz
- Host interface
  - Synchronous serial interface (SPI interface is supported)
  - Command control
- 16-bit full-digital amplifier
  - Sampling rate (fs): 16, 11.025 and 8 kHz
  - Digital Input: 16 bits
  - Operating voltage: 3.3/1.8V
- Clock
  - 32.768KHz
- Package
  - 64-pin TQFP (10mm x 10mm) with 0.5mm-pitch pins
- Supply voltage
  - 3.3V (I/O power supply)
  - 1.8V (Core power supply)

3. Pinout Diagram (Top View)

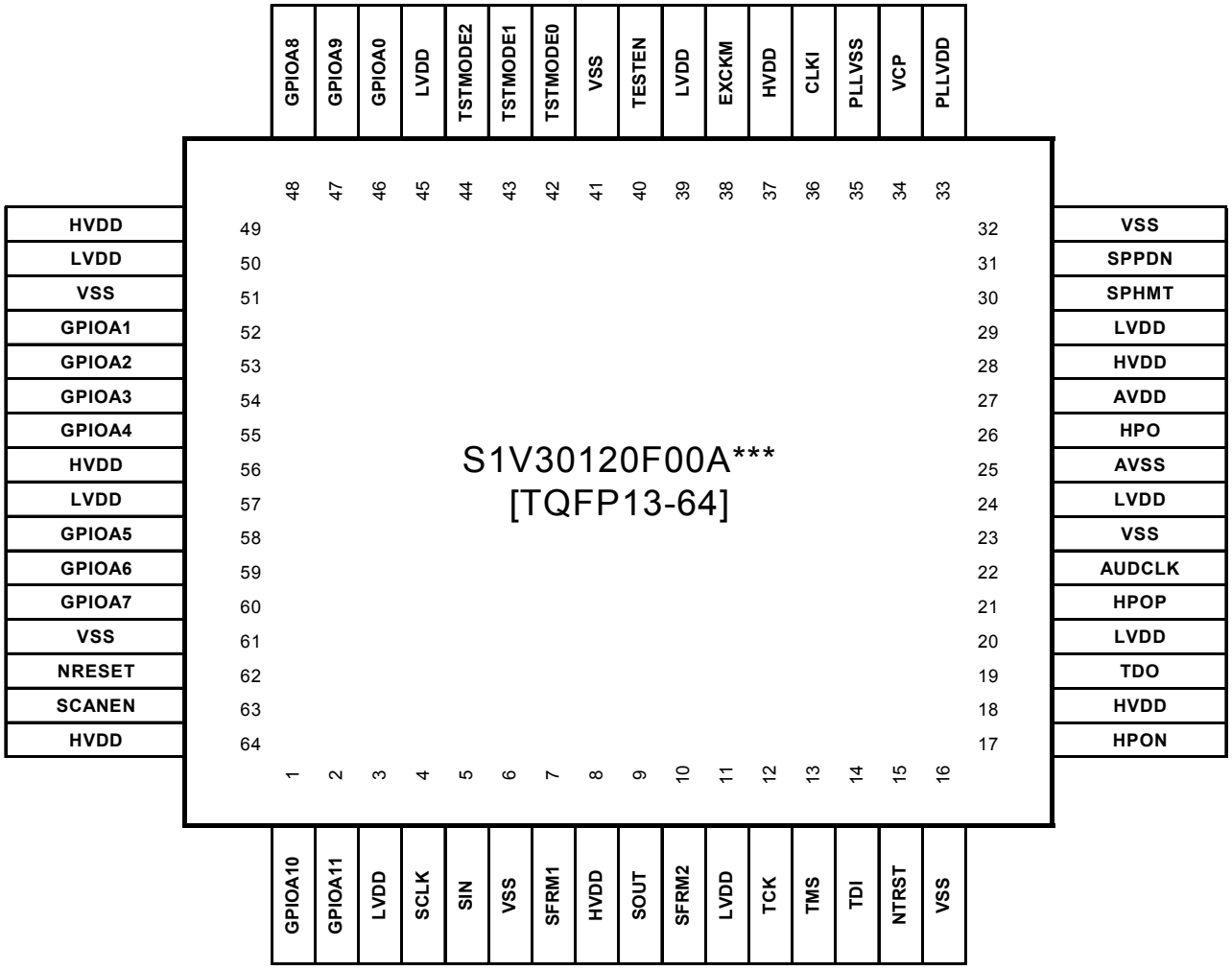


Fig. 3-1 TQFP13-64 Package Pinout

4. Pin Description

- Symbols

  I = Input pin

  O = Output pin

  IO = Bi-directional pin

  P = Power pin

  Z = High impedance

I/O cells

Symbol	Function
IC	LVCMOS input
IH	LVCMOS Schmitt-level input
ICP1	LVCMOS input with pull-up resistor （50kΩ when 3.3V (typ)）
ICD2	LVCMOS input with pull-down resistor (100kΩ when 3.3V (typ))
O1	Output buffer (2mA/-2mA output current when 3.3V (typ))
O3	Output buffer (8mA/-8mA output current when 3.3V (typ))
T1	3-state output buffer (2mA/-2mA output current when 3.3V (typ))
BC1	Bi-directional IO buffer (2mA/-2mA output current when 3.3V (typ)）
BC1P2	Bi-directional IO buffer with pull-up resistor (100kΩ when 3.3V (typ)) (2mA/-2mA output current when 3.3V(typ))
BC1D2	Bi-directional IO buffer with pull-down resistor (100kΩ when 3.3V (typ)) (2mA/-2mA output current when 3.3V (typ))
BC3D2	Bi-directional IO buffer with pull-down resistor (100kΩ when 3.3V (typ)) (8mA/-8mA output current when 3.3V(typ))
LOT	Transparent Output
ITST1	Test input with pull-down resistor (120kΩ when 1.8V (typ))

Clock synchronous serial interface

Pin Name	Pin	I/O	I/O Cell Type	RESET# State	Power	Pin Description
SIN	5	IO	BC1	Z	HVDD	Serial data input
SCLK	4	IO	BC1	Z	HVDD	Serial clock input
SFRM1	7	IO	BC3P2	Z	HVDD	Slave device select input
SOUT	9	IO	BC3P2	Pull-up	HVDD	Serial data output
SFRM2	10	IO	O3	L	HVDD	Master device select output

GPIO

Pin Name	Pin	I/O	I/O Cell Type	RESET# State	Power	Pin Description
GPIOA[11:0]	2,1,47,48,60,59,58, 55,54,53,52,46	IO	BC1D2	Pull-down	HVDD	General-purpose IO port

4. Pin Description

Full-digital audio amplifier

Pin Name	Pin	I/O	I/O Cell Type	RESET# State	Power	Pin Description
HPO	26	O	LOT	L	AVDD	Audio output
HPON	17	O	O1	L	HVDD	Inverted, unbuffered –digital- version of HPO
AUDCLK	22	O	O1	L	HVDD	Audio PWM clock
HPOP	21	O	O1	H	HVDD	Unbuffered –digital- version of HPO
SPPDN	31	O	O1	L	HVDD	Open in normal operation
SPHMT	30	O	O1	L	HVDD	Audio output in output period (Low active)

Clock/Reset

Pin Name	Pin	I/O	I/O Cell Type	RESET# State	Power	Pin Description
CLKI	36	I	IC	Z	HVDD	Reference clock input (32.768kHz)
NRESET	62	I	IH	Z	HVDD	Reset input (Low active)

Test

Pin Name	Pin	I/O	I/O Cell Type	RESET# State	Power	Pin Description
TSTMODE[2:0]	44, 43, 42	I	IC	Z	HVDD	Test pin (Set to low in normal operation)
TESTEN	40	I	ITST1	Pull-down	LVDD	Test pin (Set to low in normal operation)
SCANEN	63	I	IBD2	Pull-down	HVDD	Test pin (Set to low in normal operation)
EXCKM	38	I	IC	Z	HVDD	Test pin (Set to low in normal operation)
NTRST	15	I	IH	Z	HVDD	Test pin (Set to low in normal operation)
TDI	14	I	ICP1	Pull-up	HVDD	Test pin (Set to high in normal operation)
TMS	13	I	ICP1	Pull-up	HVDD	Test pin (Set to high in normal operation)
TCK	12	I	ICP1	Pull-up	HVDD	Test pin (Set to high in normal operation)
TDO	19	O	T1	Z	HVDD	Test pin (Open in normal operation)
VCP	34	O	LOT	Z	PLLVDD	Test pin (Open in normal operation)

Power supply

Pin Name	Pin	I/O	Pin Description
HVDD	8,18,28,37,49,56,64	P	Power supply for I/O buffers (3.3V)
LVDD	3,11,20,24,29,39,45,50,57	P	Power supply for the internal circuit (1.8V)
PLLVDD	33	P	Power supply for PLL (1.8V)
AVDD	27	P	Power supply for full-digital amplifier (1.8V / 3.3V)
VSS	6,16,23,32,41,51,61	P	GND (I/O, internal circuit)
PLLVSS	35	P	GND (PLL)
AVSS	25	P	GND (Full-digital amplifier)

5. Function Description

5.1 Typical Application System

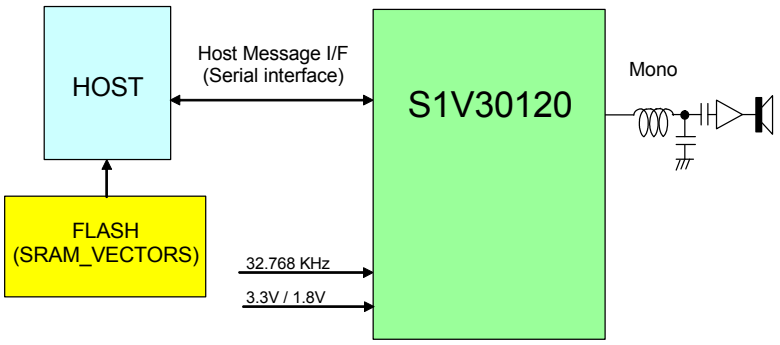


Fig. 5-1 Standard Application system

Fig. 5-1 illustrates a typical application system using the S1V30120. The host processor communicates with the S1V30120 over the serial interface, using commands (message protocol) to control the embedded algorithms. For more information on commands, see "S1V30120 Message Protocol Specification."

On reset the S1V30120 runs the bootstrap loader firmware. The host must then use bootstrap loader messages to load the SRAM firmware contents and ROM firmware updates (SRAM_VECTORS) into the S1V30120 device's SRAM and to switch to running the main mode. These SRAM_VECTORS are stored in FLASH in the typical application system shown in Fig. 5-1 above.

Refer to section 4 of the S1V30120 message protocol specification for details of the bootstrap loader messages and section 5 for details of the the main mode messages.

6. Electrical Characteristics

6.1 Absolute Maximum Rating

(VSS=0[V])

Parameter	Symbol	Rated Value	Unit
Supply voltage	HVDD	VSS-0.3 ~+4.0	V
	LVDD	VSS-0.3~+2.5	V
	PLLVDD	VSS-0.3 ~ +2.5	V
	AVDD	VSS-0.3 ~ +4.0	V
Input voltage	HVI	VSS-0.3 ~ HVDD+0.5	V
	LVI	VSS-0.3 ~ LVDD+0.5	V
Output voltage	HVO	VSS-0.3 ~ HVDD+0.5	V
	AVO	VSS-0.3 ~ HVDD+0.5	V
Output current/pin (Except HPO)	IOUT	±10	mA
Storage temperature	Tstg	-65 ~ +150	°C

6.2 Recommended Operating Conditions

(VSS=0[V])

Parameter	Symbols	Min.	Typ.	Max.	Unit
Supply voltage	HVDD	3.00	3.30	3.60	V
	LVDD	1.65	1.80	1.95	V
	PLLVDD	1.65	1.80	1.95	V
	AVDD	1.65	1.80	1.95	V
		3.00	3.30	3.60	
Input voltage	HVI	VSS	-	HVDD	V
	LVI	VSS	-	LVDD	V
Ambient temperature	Ta	-40	25	85	°C

Take the following sequences for powering on or off the IC:

(When AVDD=1.8V)

Power on: LVDD/PLLVDD/AVDD => HVDD
Power off: HVDD => LVDD/PLLVDD/AVDD

(When AVDD=3.3V)

Power on: LVDD/PLLVDD => HVDD/AVDD
Power off: HVDD/AVDD => LVDD/PLLVDD

Notes:

– Do not apply voltage only to HVDD longer than a second with LVDD, PLLVDD and AVDD turned off, or the product reliability may be harmed.

– When returning HVDD from the off-state to the on-state, the state of the internal circuit is not guaranteed due to power supply noise, etc. Therefore, be sure to initialize the circuit by NRESET after the IC power-up.

6.3 DC Characteristics

The DC input characteristics (based on Section 6.2 Recommended Operating Conditions)

Parameter		Symbol	Condition	Min.	Typ.	Max.	Unit
Supply current							
	Supply current[1]	IDDH	HVDD=3.3V	-	0.05	-	mA
		IDDL	LVDD=1.8V	-	20.0	-	mA
		IDDP	PLLVDD=1.8V	-	1.5	-	mA
		IDDAL	AVDD=1.8V, no load	-	0.4	-	mA
		IDDAH	AVDD=3.3V, no load	-	1.0	-	mA
Static current							
	Supply current[2]	IDDSH	VIN = HVDD or VSS	-	2.0	-	µA
		IDDSL	HVDD=3.6V	-	5.0	-	µA
		IDDSP	LVDD=PLLVDD=1.95V	-	0.2	-	µA
		IDDSA	AVDD=3.6V	-	0.3	-	µA
Input leakage							
	Input leakage current	IL	HVDD=3.6V LVDD=1.95V PLLVDD=1.95V AVDD=3.6V HVIH=HVDD LVIH=LVDD VIL=VSS	-5	-	5	µA

1: Approximate current values during the Text to Speech Synthesis under the recommended operating conditions (Ta=25°C)
2: Static current under the recommended operating conditions (Ta=25°C)

The DC input characteristics (based on Section 6.2, Recommended Operating Conditions) (Continued)

Parameter		Symbol	Condition	Min.	Typ.	Max.	Unit
Input characteristic (LVCMOS)		Pin names: SIN, SCLK, SFRM1, SOUT, GPIOA[11:0], CLKI, TSTMODE[2:0], SCANEN, EXCKM, TDI, TMS, TCK					
	H-level input voltage	HVIH	HVDD=3.6V	2.2	-	-	V
	L-level input voltage	HVIL	HVDD=3.0V	-	-	0.8	V
Input characteristic (LVCMOS)		Pin name: TESTEN					
	H-level input voltage	LVIH	LVDD=1.95V	1.27	-	-	V
	L-level input voltage	LVIL	LVDD=1.65V	-	-	0.57	V
Schmitt input characteristic (LVCMOS)		Pin names: NRESET, NTRST					
	H-level input voltage	VT+	HVDD=3.6V	1.4	-	2.7	V
	L-level input voltage	VT-	HVDD=3.0V	0.6	-	1.8	V
	Hysteresis voltage	ΔV	HVDD=3.0V	0.3	-	-	V
Input characteristic		Pin name: TDI, TMS, TCK					
	Pull-up resistance	RPU1	VI=VSS	25	50	120	kΩ
Input characteristic		Pin name: SFRM1,SOUT					
	Pull-up resistance	RPU2	VI=VSS	50	100	240	kΩ
Input characteristic		Pin name: GPIOA[11:0], SCANEN					
	Pull-down resistance	RPD1	VI=HVDD	50	100	240	kΩ
Input characteristic		Pin name: TESTEN					
	Pull-down resistance	RPD2	VI=LVDD	48	120	300	kΩ

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Output characteristic	Pin names: SIN, SCLK, GPIOA[11:0], AUDCLK, HPOP, SPPDN, SPHMT TDO, HPON					
H-level output voltage	VOH1	HVDD=3.0V IOH=-2mA	HVDD-0.4	-	-	V
L-level output voltage	VOL1	HVDD=3.0V IOL=2mA	-	-	VSS+0.4	V
Output characteristic	Pin name: SOUT,SFRM1,SFRM2					
H-level output voltage	VOH2	HVDD=3.0V IOH=-8mA	HVDD-0.4	-	-	V
L-level output voltage	VOL2	HVDD=3.0V IOL=8mA	-	-	VSS+0.4	V
Output characteristic	Pin names: SIN, SCLK, SFRM1, SFRM2, SPPDN, SPHMT, AUDCLK, HPOP, HPON, SOUT, GPIOA[11:0], TDO					
Off-state leakage current	IOZ	HVDD=3.6V HVOH=HVDD VOL=VSS	-5	-	5	µA

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Output characteristic	Pin names: All input pins					
Input pin capacitance	CI	f=1MHz HVDD=LVDD=AVDD= PLLVDD=0V	-	-	8	pF
Pin capacitance	Pin names: All output pins except HPO					
Output pin capacitance	CO1	f=1MHz HVDD=LVDD=AVDD= PLLVDD=0V	-	-	8	pF
Pin capacitance	Pin names: All output pins					
I/O pin capacitance	CIO	f=1MHz HVDD=LVDD=AVDD= PLLVDD=0V	-	-	8	pF

6.4 AC Characteristics

6.4.1 Clock Timing

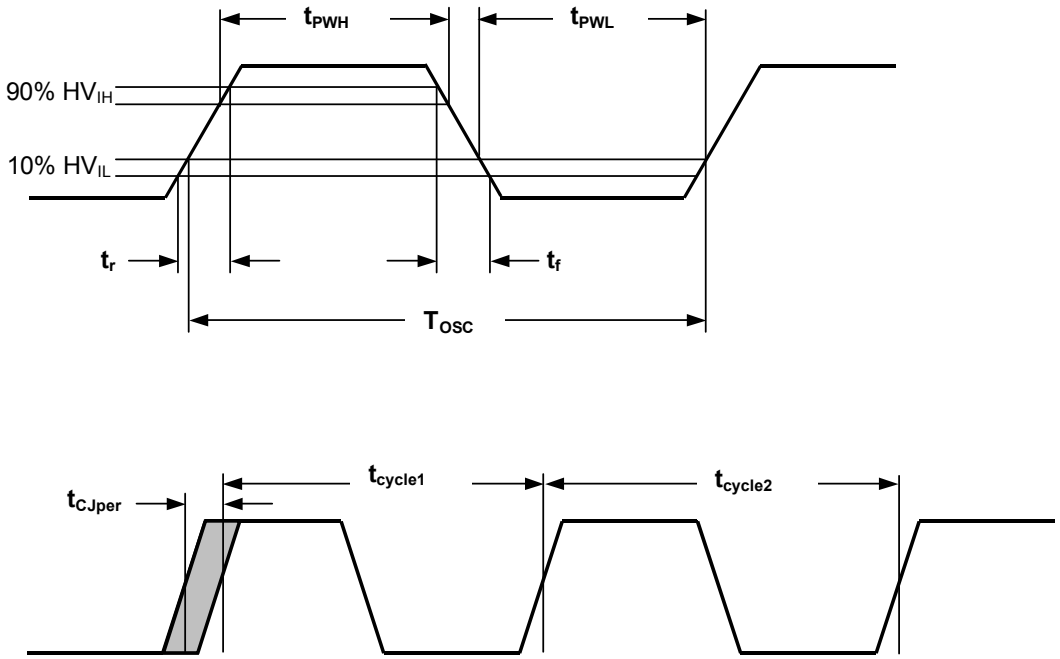


Fig. 6-1 Clock Timing

Symbol	Parameter	Min.	Typ.	Max.	Unit
f_{OSC}	Input clock frequency	-	32.768	-	kHz
T_{OSC}	Input clock period	-	1/fosc	-	µs
t_{pwh}	Input clock pulse width high	5	-	-	µs
$t_{pw\ 1}$	Input clock pulse width low	5	-	-	µs
t_r	Input clock rising time (10% ->90%)	-	-	12	µs
t_f	Input clock falling time (90%->10%)	-	-	12	µs
t_{CJper}	Input clock period jitter (*2, 4)	-10	-	10	ns
$t_{CJcycle}$	Input clock cycle jitter (*1, 3, 4)	-10	-	10	ns
*1	$t_{CJcycle} = t_{cycle1} - t_{cycle2}$				
*2	The input clock period jitter is the displacement relative to the center period (reciprocal of center frequency).				
*3	The input clock cycle jitter is difference in period between adjacent cycles.				
*4	The jitter characteristics must meet both t_{Cjper} and $t_{Cjcycle}$ characteristics.				

6.4.2 Initialization Timing

6.4.2.1 Power-on/Reset Timing

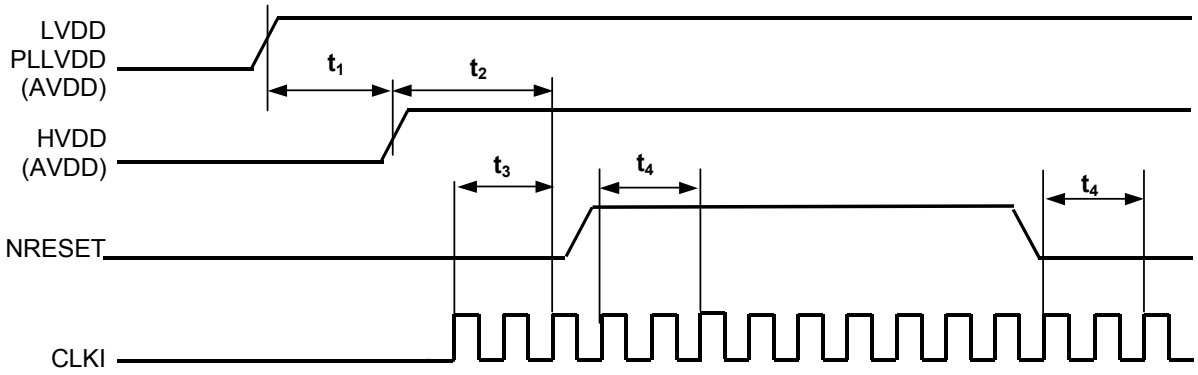


Fig. 6-2 Power-on/Reset Timing

Symbol	Parameter	Min.	Max.	Unit
t_1	Delay from the LVDD and PLLVDD (AVDD) power-on to HVDD (AVDD) power-on*1	10	-	µs
t_2	Minimum delay from the HVDD power-on to theCLK1 rising edge before NRESET release	100	-	µs
t_3	The minimum RESET assertion on system power up	2	-	T_{OSC}*2
t_4	NRESET synchronization time (Number of clock cycles before NRESET is applied internally)	2	-	T_{OSC}*2
*1	See Section 6.2 Recommended Operating Conditions.			
*2	T_{OSC} is the CLKI clock period.			

6.4.2.2 Power-off Sequence

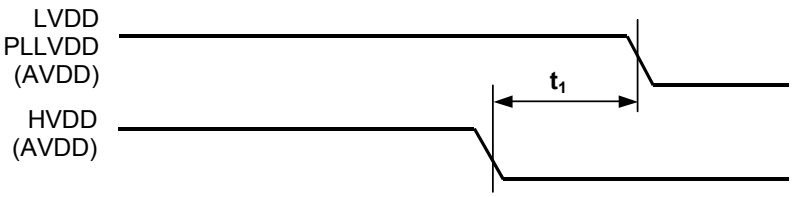


Fig. 6-3 Power-off Sequence

Symbol	Parameter	Min.	Max.	Unit
t_1	Delay from HVDD (AVDD) power-off to LVDD and PLLVDD (AVDD) power-off *1.	-	500	µs
*1	See Section 6.2, Recommended Operating Conditions.			

6.4.3 Clock Synchronous Serial Interface (SPI)

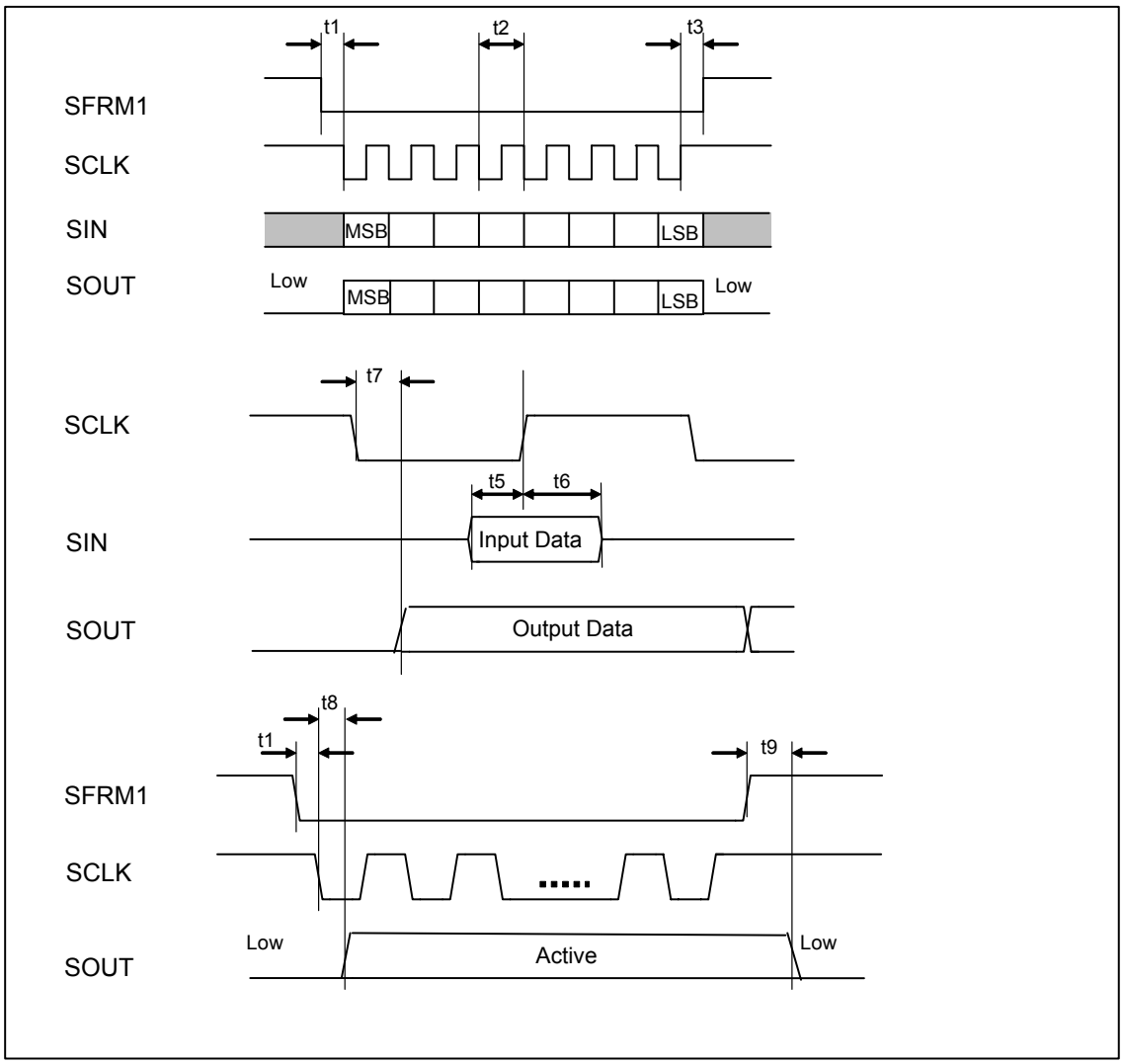


Fig. 6-4 Clock Synchronous Serial Interface

Symbol	Parameter	Min.	Max.	Unit
t_1	SFRM1 falling time to SCLK falling time	200	-	ns
t_2	SCLK cycle time	1.0	-	µs
t_3	SCLK rising time to SFRM1 rising time	200	-	ns
t_5	SIN setup time	10	-	ns
t_6	SIN hold time	200	-	ns
t_7	SCLK falling time to SOUT going active	-	200	ns
t_8	SCLK falling time to SOUT going active with SFRM1=L	-	200	ns
t_9	SFRM1 rising time to SOUT going Low	-	250	ns

6.5 Full-Digital Audio Amplifier

The electrical characteristics of the full-digital audio amplifier are as follows unless otherwise noted:

- Ta = 25°C
- HVDD = 3.3V, LVDD = 1.8V, PLLVDD = 1.8V
- Input signal frequency = 1kHz
- Input signal level = 0dBFS
- fs = 32kHz
- Test frequency range= 20Hz ~16kHz
- Load impedance = 16Ω
- Connection to the 2nd low-pass filter to the output (HPO)

When AVDD = 1.8V

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Load impedance	R_L		16	-	-	Ω
Output power	P_o		2	3	-	mW
Total harmonic distortion	THD+N	Input signal level = -6dBFS	-	0.13	0.25	%
Signal noise ratio	SNR		73	76	-	dB

When AVDD = 3.3V

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Load impedance	R_L		16	-	-	Ω
Output power	P_o		8	11	-	mW
Total harmonic distortion	THD+N	Input signal level = -6dBFS	-	0.1	0.15	%
Signal noise ratio	SNR		79	82	-	dB

- Full Digital Amplifier characteristic may be deteriorated by AVDD Voltage fluctuation. Use stable power supplies for AVDD.

7. External Connection Example

7.1 Connection Example: Clock Synchronous Serial Interface

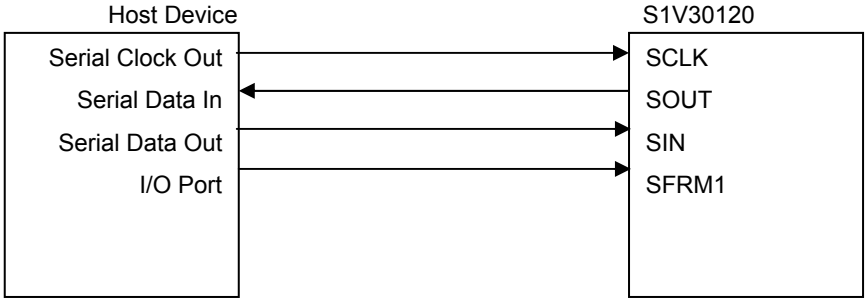
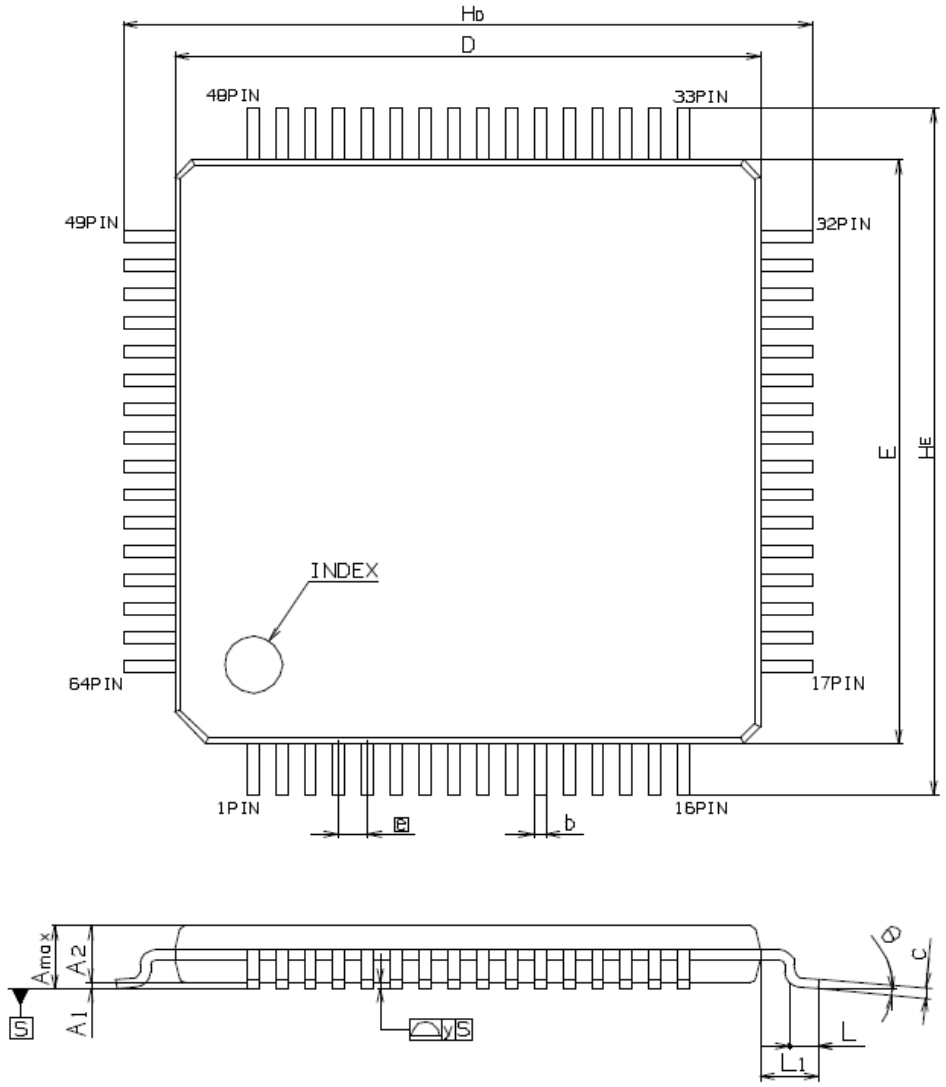


Fig. 7-1 Clock Synchronous Serial Interface Connection Example

Note:

When SFRM1 is Low, SOUT goes active. When SFRM1 is High, SOUT goes Low.

8. Package Dimensions



Symbol	Dimension in Millimeters		
	Min	Nom	Max
E	-	10	-
D	-	10	-
A_{max}	-	-	1.2
A_1	-	0.1	-
A_2	-	1	-
e	-	0.5	-
b	0.17	-	0.27
c	0.09	-	0.2
θ	0°	-	10°
L	0.3	-	0.75
L_1	-	1	-
H_E	-	12	-
H_D	-	12	-
y	-	-	0.08

Fig. 8-1 S1V30120F00A* Dimensions**

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